

In re Application of: John Kemeny  
Attorney Docket No.: EMR-002.01

AMENDMENTS TO THE CLAIMS

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Claims 1-30 (Canceled).

31. (Previously presented) A method comprising:

representing a plurality of memory addresses associated with at least one storage device as a plurality of hierarchical branches in a trie data structure;

receiving a request for data stored at a particular one of the memory addresses of the at least one storage device;

traversing at least some of the hierarchical branches in the trie data structure using different portions of the particular one of the memory addresses storing the requested data;

identifying a memory address associated with a cache memory based on the traversal, the identified cache memory address being stored in a leaf of the trie data structure; and

transmitting data stored at the identified cache memory address in response to the request.

32. (New) The method of claim 31, wherein the trie data structure comprises a multi-dimensional array, wherein an index of a dimension of the array corresponds to different trie data structure branches.

33. (New) The method of claim 32, wherein traversing the trie data structure comprises, repeatedly, indexing into the dimension of the array using the different portions of the particular one of the memory addresses.

34. (New) The method of claim 31, wherein traversing the trie data structure using the different portions of the particular one of the memory addresses comprises

performing an operation on at least one of the different portions of the particular one of the memory addresses; and

traversing the trie data structure using the operation results.

35. (New) The method of claim 31, wherein the cache memory address associated with the particular one of the memory addresses dynamically changes.

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36. (New) A data storage system, comprising:

- (a) at least one storage device;
- (b) a cache memory;
- (c) instructions for causing a processor to:
  - (1) represent a plurality of memory addresses associated with the at least one storage device as a plurality of hierarchical branches in a trie data structure;
  - (2) receive a request for data stored at a particular one of the memory addresses of the at least one storage device;
  - (3) traverse at least some of the hierarchical branches in the trie data structure using different portions of the particular one of the memory addresses storing the requested data;
  - (4) identify a memory address associated with the cache memory based on the traversal, the identified cache memory address being stored in a leaf of the trie data structure; and
  - (5) transmit data stored at the identified cache memory address in response to the request.

37. (New) The data storage system of claim 36, wherein the instructions for causing the processor to traverse the trie data structure based on the different portions of the particular one of the memory addresses comprise instructions for causing the processor to:

- perform an operation on at least one of the different portions of the particular one of the memory addresses the first address; and
- traverse the trie data structure using the operation results.

38. (New) The data storage system of claim 36, wherein the cache memory address associated with the particular one of the memory addresses dynamically changes.

39. (New) A computer program product, disposed on a computer readable medium, the computer program product including instructions for causing a processor to:

- represent a plurality of memory addresses associated with at least one storage device as a plurality of hierarchical branches in a trie data structure;

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receive a request for data stored at a particular one of the memory addresses of the at least one storage device;

traverse at least some of the hierarchical branches in the trie data structure using different portions of the particular one of the memory addresses storing the requested data;

identify a memory address associated with a cache memory based on the traversal, the identified cache memory address being stored in a leaf of the trie data structure; and

transmit data stored at the identified cache memory address in response to the request.

40. (New) The computer program product of method of claim 39, wherein the trie data structure comprises a multi-dimensional array, wherein an index of a dimension of the array corresponds to different trie data structure branches.

41. (New) The computer program product of claim 40, wherein the instructions for causing the processor to traverse the trie data structure comprise instructions for causing the processor to, repeatedly, index into the dimension of the array using the different portions of the particular one of the memory addresses.

42. (New) The computer program product of claim 39, wherein the instructions for causing the processor to traverse the trie data structure using the different portions of the particular one of the memory addresses comprises instructions for causing the processor to:

perform an operation on at least one of the different portions of the particular one of the memory addresses; and

traverse the trie data structure using the operation results.

43. (New) The computer program product of claim 39, wherein the cache memory address associated with the particular one of the memory addresses dynamically changes.